UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,190	02/13/2002	Kenneth Y. Ng	884.A25US1	5309

7590 05/19/2005

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,190	NG, KENNETH Y.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-28 and 30-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-28 and 30-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 03/24/2005.

2. Claims 1-10, 12-28, and 30-40 are pending in this application. Claims 1, 5, 13, 22, 25, 30, and 37 are independent claims. In Amendment, claims 11 and 29 are cancelled; and claims 5, 25, 32 and 37 are amended. This Office Action is made final.

Drawings

3. Figures 2, 3, and 5 should be designated by a legend such as --Prior Art-- because these Figures are disclosed in Figures 2 and 4-5 respectively in U.S. Patent No. 6,301,599. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 5-10 and 12-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Chehrazi et al. (U.S. 6,301,599).

Re claim 5, Chehrazi et al. disclose in Figure 4 a Booth encoder circuit (400) comprising: a plurality of transistors (e.g. 404-409) to receive a plurality of multiplier bits (b0-b2) and complements of plurality of multiplier bits (output of 401-403); and a plurality of logic circuits (410-414) coupled to ones of plurality of transistors to output Booth encoded signals (S0-S2 and S_1-S_2) wherein Booth encoded signals are substantially delay-matched at an output of Booth encoder circuit (e.g. output signals from encoder circuit in Figure 4 wherein all output signals S0, S1, S_1, S2, and S_2 are aligned with gate delay and col. 8 claim 13).

Re claim 6, Chehrazi et al. further disclose in Figures 2 and 4-5 plurality of transistors comprise a first sub-circuit (circuit for generating S1 and S_1 in Figure 4), a second sub-circuit (circuit for generating S2 in Figure 4), a third sub-circuit (circuit for generating S_2 in Figure 4), and a fourth sub-circuit (circuit for generating S0 in Figure 4), and plurality of Logic circuits comprise first Logic circuits, second Logic circuits, third logic circuit and fourth logic circuits (Figure 4), first sub-circuit to receive two of multiplier bits and complements of two multiplier bits , first sub-circuit to provide a

signal to first logic circuits, first logic circuits to output two Booth encoded signals (S1 and S_1 in Figure 4).

Re claim 7, Chehrazi et al. further disclose in Figures 2 and 4-5 second sub-circuit to receive one of multiplier bits and complements of two multiplier bits, second sub-circuit to provide a signal to second Logic circuits, second Logic circuits to output one Booth encoded signal (S2 in Figure 4).

Re claim 8, Chehrazi et al. further disclose in Figures 2 and 4-5 third sub-circuit to receive two of multiplier bits and complements of one multiplier bit, third sub-circuit to provide a signal to third Logic circuits, third Logic circuits to output one Booth encoded signal (S_2 in Figure 4).

Re claim 9, Chehrazi et al. further disclose in Figures 2 and 4-5 fourth sub-circuit to receive two of multiplier bits and complements of two multiplier bits, and to provide a signal to fourth Logic circuits based on two of multiplier bits and complements of two multiplier bits, fifth sub-circuit to receive two of multiplier bits and complements of two multiplier bits and to provide a signal to fourth logic circuit based on two of multiplier bits and complements of two multiplier bits, fourth Logic circuit to output one Booth encoded signal (S0 in Figure 4).

Re claim 10, Chehrazi et al. further disclose in Figures 2 and 4-5 Booth encoded signals represent a multiply by zero; a multiply by one; a multiply by negative one, a multiply by two; and a multiply by negative two (col. 2 lines 30-33).

Re claim 12, Chehrazi et al. further disclose in Figures 2 and 4-5 circuit has a maximum of a three-gate delay from an input of Booth encoder circuit to an output of Booth encoder circuit (e.g. Figure 4 with 401, 405 and 413).

Re claim 13, it has same limitation cited in claim 12. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 14, Chehrazi et al. further disclose in Figures 2 and 4-5 logic comprises a plurality of transistors (e.g. 404-409), a plurality of NAND gates (412-414) and a plurality of inverters (e.g. 401-403).

Re claim 15, Chehrazi et al. further disclose in Figures 2 and 4-5 NAND gates comprises two-input NAND circuits (e.g. 412-414).

Re claim 16, it has same limitation cited in claim 6. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 17, it has same limitation cited in claim 7. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 18, it has same limitation cited in claim 8. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 19, it has same limitation cited in claim 9. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 20, it has same limitation cited in claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 21, it has same limitation cited in claim 11. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 22, Chehrazi et al. further disclose in Figures 2 and 4-5 a circuit comprising logic to receive a plurality of multiplier bits and complements of multiplier bits (e.g. b0-b2 and its complements from 401-403 in Figure 4), logic including a plurality of transistors (e.g. 404-409), a plurality of NAND gates (e.g. 412-414) and a plurality of inverters (e.g. 401-403) configured to output delay-matched Booth encoded signals (claim 13 in col. 8) based on multiplier bits and complements.

Re claim 23, it has same limitation cited in claim 12. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 24, it has same limitation cited in claim 15. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

Re claim 25, it has same limitation cited in claim 9. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 26, it has same limitation cited in claim 12. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 27, it has same limitation cited in claim 14. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Re claim 28, it has same limitation cited in claim 15. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

6. Claims 30-31 and 33-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. 5,818,743).

Re claim 30, Lee et al. further disclose in Figure 9A partial products generator circuit (e.g. 280) comprising: a first multiplexing device (e.g. first mux of 244') having a plurality of first transistors to receive Booth encoded signals (output of Booth Encoder on the left of Figure 9A) and to provide a first partial products output (output of the first mux into FA); and a second multiplexing device (e.g. first mux of 244'') having a plurality of second transistors to receive Booth encoded signals (e.g output of Booth Encoder on the left of Figure 9A) and multiplexed data from first multiplexing device and to provide a second partial products output (e.g. output of the first mux into FA of 244'').

Re claim 31, Lee et al. further disclose in Figure 9A a third multiplexing device having a plurality of third transistors to receive Booth encoded signals and multiplexed data from second multiplexing device and to provide a third partial products output (e.g. 244''').

Re claim 33, Lee et al. further disclose in Figure 9A first multiplexing device further to receive a signal corresponding to a first bit of a multiplicand and a signal corresponding to a complement of first bit (e.g. multiplicand and bar(multiplicand)).

Re claim 34, Lee et al. further disclose in Figure 9A second multiplexing device further to receive a signal corresponding to a second bit of multiplicand and a signal corresponding to a complement of second bit (e.g. multiplicand and bar(multiplicand)).

Re claim 35, Lee et al. further disclose in Figure 9A plurality of first transistors comprise five transistors (input into mux).

Re claim 36, Lee et al. further disclose in Figure 9A multiplexed data comprises data from a previous bit of a multiplicand (e.g. second line of mux in 244'').

Re claim 37, it has same limitation cited in claim 36. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 36.

Re claim 38, Lee et al. further disclose in Figure 9A previous multiplexing device receives Booth encoded signals and provides a second partial products output for a second bit of multiplicand based at Least on multiplexed data from another multiplexing device (e.g. second line of mux in 244'').

Re claim 39, it has same limitation cited in claim 33. Thus, claim 39 is also rejected under the same rationale as cited in the rejection of rejected claim 33.

Re claim 40, it has same limitation cited in claim 34. Thus, claim 40 is also rejected under the same rationale as cited in the rejection of rejected claim 34.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being obvious over Chehrazi et al. (U.S. 6,301,599) in view of Lee et al. (U.S. 5,818,743).

Re claim 1, Chehrazi et al. disclose in Figures 2 and 4-5 a circuit comprising a booth encoder circuit (202 in Fig. 2) having a plurality of transistors (e.g. 404 in Fig. 4) to receive a plurality of multiplier bits (e.g. b0-b2) and complements of plurality of multiplier bits (e.g. output of 401-403), and a plurality of Logic circuits (e.g. 410-414)

coupled to ones of plurality of transistors to output Booth encoded signals (e.g. S0-S_2); and a partial products generating circuit (e.g. 204 in Fig. 2) having a multiplexing device (e.g. 506) to receive Booth encoded signals and to provide partial products output (col. 6 lines 15-20). Chehrazi et al. do not clearly disclose the partial products generating circuit having a first and second multiplexing device to generate first and second partial products respective base on the Booth encoded signals and previous output even thought Chehrazi et al. disclose in column 2 lines 38-43 that the partial products generating circuits are function as a multiplexer as conventional. However, Lee et al. disclose in Figure 9A the partial products generating circuit (280) having a first multiplexing device (e.g. mux in 244') to receive Booth encoded signals (e.g. Booth Encoder) and to provide first partial products output (output of 244'), and a second multiplexing device (e.g. 244'') to receive Booth encoded signals (e.g. Booth Encoder) and multiplexed data from first multiplexing device (e.g. second mux from left in 244'') and to provide a second partial products output (output of 244''). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a first and second multiplexer to generate a first and second partial products based on receiving the Booth encoder signal and the previous output as seen in Leet al.'s invention into Chehrazi et al.'s invention because it would enable to speed up the multiplication by reducing the number of partial products needed to be generated and added in the multiplier (col. 3 lines 65-67 and col. 4 lines 1-2).

Re claim 2, Chehrazi et al. further disclose in Figures 2 and 4-5 plurality of Logic circuits includes a recoding circuit (col. 2 lines 37-42 wherein the multiplexing process as the recoding circuit to generate the partial products).

Re claims 3-4, Chehrazi et al. do not disclose in Figures 2 and 4-5 first multiplexing device further to receive a signal corresponding to a first bit of a multiplicand and a signal corresponding to a complement of first bit and respectively for second bit. However, Chehrazi et al. disclose in Figure 4 first multiplexing device further to receive a signal corresponding to a first bit of a multiplicand and a signal corresponding to a complement of first bit (e.g. multiplicand and bar(multiplicand)) and respectively for second bit. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add first multiplexing device further to receive a signal corresponding to a first bit of a multiplicand and a signal corresponding to a complement of first bit and respectively for second bit as seen in Leet al.'s invention into Chehrazi et al.'s invention because it would enable to speed up the multiplication by reducing the number of partial products needed to be generated and added in the multiplier (col. 3 lines 65-67 and col. 4 lines 1-2).

9. Claim 32 is rejected under 35 U.S.C. 103(a) as being obvious over Lee et al. (U.S. 5,818,743).

Re claim 32, Lee et al. do not disclose in Figure 9A pluralities of first transistors comprise NFET transistors. However, the examiner takes an official notice that the NFET transistors are known in the art for used in multiplier. Therefore, it would have

been obvious to a person having ordinary skill in the art at the time the invention is made to add the NFET transistors into the multiplier in Lee et al.'s invention because it would enable to increase the system performance by reducing the delay between gates.

Response to Arguments

10. Applicant's arguments filed 03/24/2005 have been fully considered but they are not persuasive.

a. The applicant argues in page 9 for claims 5-10 and 12 that the cited reference by Chehrazi does not disclose the Booth encoded signals are substantially delay-matched at an output as cited in the claimed invention.

The examiner respectfully submits that the Figure 4 clearly shows the output Booth encoded signals are substantially generated or delay-matched. The first three output signals (S0, S1, and S_1) are generated or outputted at the same time while the other signals (S2 and S_2) are substantially generated or outputted same time with the first three output signals.

b. The applicant argues in page 9 for claims 13-21 that the cited reference by Chehrazi does not disclose a logic configured to have a maximum of three gate delays from an input of multiplier circuit to an output of multiplier circuit as cited in the claimed invention.

The examiner respectfully submits that Figure 4 clearly shows the maximum of three gate delays as the signal path from b1 to 402; 402 to 405; and 405 to 412.

The three gate delays are inverter gate (402), the transistor gate (405), and the NAND gate (412).

c. The applicant argues in page 10 for claims 22-24 that the cited reference by Chehrazi does not disclose the output delay-matched Booth encoded signals.

The examiner respectfully submits that the Figure 4 clearly shows the output Booth encoded signals are substantially generated or delay-matched. The first three output signals (S0, S1, and S_1) are generated or outputted at the same time while the other signals (S2 and S_2) are substantially generated or outputted same time with the first three output signals.

d. The applicant argues in page 10 for claims 25-28 that the cited reference by Chehrazi does not disclose the second subcircuit to provide a signal to second logic circuits, or said third subcircuit to provide a signal to third logic circuits as cited in the claimed invention.

The examiner respectfully submits that Figure 4 clearly shows the second subcircuit to provide a signal to second logic circuits (e.g. S1), or said third subcircuit to provide a signal to third logic circuits (e.g. S_1).

e. The applicant argues in page 10 for claims 30-31 and 33-40 that the cited reference by Lee does not disclose a second multiplexing device having a plurality of second transistors to receive said Booth encoded signals and multiplexed data from said

first multiplexing device and to provide a second partial products output and a multiplexing device to receive Booth encoded signals and to provide a first partial product output for a first bit of a multiplicand based at least on multiplexed data received from a previous multiplexing device as cited in the claimed invention.

The examiner respectfully submits that Lee clearly discloses in Figure 9A multiple multiplexers comprising a second multiplexing device having a plurality of second transistors to receive said Booth encoded signals and multiplexed data from said first multiplexing device and to provide a second partial products output and a multiplexing device to receive Booth encoded signals and to provide a first partial product output for a first bit of a multiplicand based at least on multiplexed data received from a previous multiplexing device.

f. The applicant argues in page 11 for claims 1-4 that the Applicant is unable to find in the proposed combination of Chaharzi and Lee.

The examiner respectfully submits that the obvious motivation is drawn from a person having ordinary skill in the art at the time the invention is made to combine the lacking feature(s) in Lee to Chaharzi's invention in order to speed up the multiplication process.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

May 12, 2005